AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 29 on pages 9-10 with the following amended paragraph:

[029] The signal swing thus developed must be carefully limited so that the pMOS devices ~~412,~~ 414, ~~and~~ 416, and 418 have sufficient drive to pull the bitline back up to V_{dd} when the memory cell 202 is turned off, or the next memory cell might impress opposite data on the other bitline. This is achieved by nMOS transistor 502 which tracks the effect of the transfer gate 402 or 404 on the bitline, thereby matching the memory cell transfer gate 402 which is in saturation while delivering constant current at a PVT point. The pMOS transistor 504 emulates the effects of the loads of pMOS transistors ~~412,~~ 414, ~~and~~ 416, and 418 on the bitline when these devices are operated in the linear region. The pMOS transistors 506, 508 and nMOS transistors 510, 512 are configured to provide a current mirror that has sufficient gain to increase the output drive of the reference since it is necessary to drive a multiplicity of bitline loads. The nMOS transistor 514 improves the stability of the circuit. Other embodiments of the circuitry for generation of V_R are possible, as will be understood by those of skill in the art.

Please replace the Abstract with the following amended Abstract:

[031] A memory system using low impedance memory bitlines that eliminate the need for a precharge clock signal. An equilibration circuit controlled by a reference voltage is connected to the first and second bitlines of a memory cell and is operable to maintain a predetermined equilibrium condition between the first and second bit lines. The equilibration circuit is operable to generate an impedance load in the first and second bit lines at a level that allows generation of differential signals in the bit lines. ~~In an~~

~~embodiment of the invention, the equilibration circuit comprises first and second pMOS devices in series with the first and second bitlines, respectively, and a third pMOS device connected between the first and second bitlines. The gates of the first, second and third pMOS devices are connected to the reference voltage. In this embodiment, the first, second and third pMOS devices operate as resistors in the linear region of MOSFET device operation.~~ The memory cell bitlines can move from a sensed state "low" to the opposite state "high" without an intervening precharge, thereby providing a significant increase in performance.